

Application. No. 09/760,646
Amendment dated January 19, 2005
Reply to Office Action of July 19, 2004

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method for correcting the clock in ~~an~~ a digital video data stream transmitted in packets over a network, said method comprising the steps of:

a- a) placing said video packets in ~~an output~~ a FIFO memory;

b- b) outputting data from said ~~output~~ FIFO memory according to a clock rate or bit rate that is adjustable;

c- c) filtering the level of data in said ~~output~~ FIFO memory to produce a current average level and a previous average level; and

d- d) changing said adjustable clock rate or bit rate according to said current average level and said previous average level in accordance with one of the relationships:

i) when an absolute value of said current average level minus a target level is less than the absolute value of said previous average level minus said target level, then set a bit rate change value equal to a predetermined minimum bit rate change value;

ii) when said current average level is greater than said target level which is, in turn, greater than a previous FIFO level, then reverse a bit rate change direction and set said bit rate change value equal to said predetermined minimum bit rate change value;

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iii) when said current average level is less than said target level which is, in turn, less than said previous average level, then reverse said bit rate change direction and set said bit rate change value equal to said predetermined minimum bit rate change value; and

iv) when an absolute value of said average current level minus said target level is greater than an absolute value of said previous average level minus said target level, then double said bit rate change value;

whereby said output FIFO memory level is driven towards a said predetermined target level.

Claim 2 (cancelled)

Claim 3 (currently amended): The method of claim 2 1, wherein in Step d (d), the rate at which said clock is changed is limited to a maximum rate in accordance with at least one predetermined specification.